REMARKS

Claims 1-14 were canceled filing this divisional application, and claims 15-18 are pending in this application. The Examiner apparently ignored the amendment made in item 17 of the application transmittal.

Allowable Claims

Applicants gratefully acknowledge that claim 16 is merely objected to as depending from a rejected base claim, but is otherwise allowable.

Claim Objections

Claims 1 and 4 were objected to.

This objection is moot because claims 1 and 4 are no longer pending.

Double Patenting

Claims 1 and 4 were rejected under the judicially created doctrine of double patenting over claims 1 and 4 respectively of U.S. Patent No. 6,555,853.

This objection is moot because claims 1 and 4 are no longer pending.

Rejections under 35 USC §102(b)

Claims 1-5, and 15 were rejected under 35 USC §102(b) as being anticipated by Murata et al (U.S. Patent No. 5,917,211).

This objection to claims 1-5 is moot because these claims are no longer pending.

Claim 15 has been amended to "A computer readable storage medium, having thereon a computer program to modify a layout pattern of an embedded array in a semiconductor integrated circuit with basic cells arranged in a matrix, said computer program comprising an operational step of modifying layout pattern data of said embedded array by detecting and removing a portion of an impurity region in a basic cell based on layout data of contact holes, the basic cell constituting a circuit."

The Examiner alleged that claim 15 is rejected in a manner similar to claim 1 except the design stage is matched in figure 7 or modifying layout is in column 50, lines 15-30. He alleged rejecting claim 1 as follows:

> A semiconductor device having an embedded array (col. 4, lines 29-39), said embedded array having basic cells arranged in a matrix (col. 12, lines 37-49), wherein a basic cell has an impurity region part of which is removed (col. 3, lines 49-58), said part corresponding with a missing contact hole (col. 40, lines 47-67) using partial etching portion of contact hole.

Murata et al describes at col. 3, lines 49-58 as follows:

> (4) In a semiconductor integrated circuit having bonding pads formed of the same conductive layer as internal wiring and connected through openings formed in a passivation film to bonding wires, the internal wiring is formed of a composite film constructed by depositing an aluminum or an aluminum alloy film, and a transition metal film formed on the aluminum or aluminum alloy film, and the bonding pads are portions of the composite film from which portions of the transition metal film are removed to expose the corresponding portions of the aluminum or aluminum alloy film.

Despite the Examiner's allegation this description does not disclose "a basic cell has an impurity region part of which is removed." Murata et al further describes at col. 40, lines 47-67 as follows:

> The middle silicon dioxide film 51B is formed by applying silicon dioxide in a thickness in the range of 100 to 150 nm by a SOG method in a flat film, baking the film at a temperature on the order of 450 °C, and then partially removing the baked film by partial etching so that only portions thereof filling recesses in the lower silicon dioxide film 51A remain unremoved. The partial etching removes the raised portions of the lower silicon dioxide film 51A to prepare a flat surface for the upper silicon dioxide film 51C. An organic film, such as a polyimide resin film, may be substituted for the middle silicon dioxide film 51B.
>
> The upper silicon dioxide film 51C is formed to reinforce the layer insulating film 51 in a thickness in the range of 500 to 700 nm by, for example, a plasma CVD process.
>
> Contact Hole Forming Process 3
>
> Then, as shown in FIG. 33, contact holes 52 are formed in the layer insulating film 51. Each contact hole 52 has a lower portion 52A formed in the lower silicon dioxide film 51A by anisotropic etching, and an upper portion 52B formed in the upper silicon dioxide film 51c by isotropic etching. After forming the contact holes 52, the semiconductor substrate 20 carrying the elements is subjected to a heat treatment at a temperature on the order of 400 °C to mend damages caused by etching.

Despite the Examiner's allegation, this description does not disclose "said part corresponding with a missing contact hole using partial etching portion of contact hole."

Moreover the description at col. 3, lines 49-58 has nothing to do with the description at col. 40, lines 47-67.

Thus, Murata et al does not teach or suggest "A computer readable storage medium, having thereon a computer program to modify a layout pattern of an embedded array in a semiconductor integrated circuit with basic cells arranged in a matrix, said computer program comprising an

operational step of modifying layout pattern data of said embedded array by detecting and removing a portion of an impurity region in a basic cell based on layout data of contact holes, the basic cell constituting a circuit," as recited in claim 15.

For at least these reasons, claim 15 patentably distinguishes over Murata et al.

Thus, the 35 USC §102(b) rejection should be withdrawn.

It is submitted that nothing in the cited reference the features recited in each claim of the present invention. Thus all pending claims are in condition for allowance. Reconsideration of the rejections, withdrawal of the rejections and an early issue of a Notice of Allowance are earnestly solicited.

If, for any reason, it is felt that this application is not now in condition for allowance, the Examiner is requested to contact Applicant's undersigned attorney at the telephone number indicated below to arrange for an interview to expedite the disposition of this case.

In the event that this paper is not timely filed, Applicant respectfully petitions for an appropriate extension of time. The fees for such an extension or any other fees which may be due with respect to this paper, may be charged to Deposit Account No. 50-2866.

Respectfully submitted,

WESTERMAN, HATTORI, DANIELS & ADRIAN, LLP

Sadao Kinashi
Attorney for Applicant(s)
Reg. No. 48,075

SK/sg
1250 Connecticut Ave. N.W.
Suite 700
Washington, D.C. 20036
(202) 822-1100
Q:\1999\991183B\991183b amdt 1.111.doc